# Intel® 82801EB/ Intel® 82801ER I/O Controller Hub 5 (Intel® ICH5)/ I/O Controller Hub 5 R (Intel® ICH5R)

**White Paper**

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# Contents

# Revision History

| Revision Number | Description | Revision Date |
|---|---|---|
| -001 | Initial Release. | April 14, 2003 |

# 1 Overview

The Intel® 82801EB and Intel® 82801ER (ICH5 and ICH5R, respectively) are integral parts of the Intel chipsets in conjunction with the (Graphics) Memory Controller Hub. Connected to the (G)MCH through hub interface 1.5, the ICH5 provides platform features and capabilities for quality, robustness, and longevity.


ICH5 platforms enable the next generation desktop storage interface with integration of Serial ATA (SATA). The ICH5 also supports eight, high-speed USB 2.0 ports and integrates an Alert Standard Format (ASF) System Management controller for network manageability. The ICH5 includes enhancements to familiar features as well, such as support for PCI Rev 2.3 and ACPI 2.0 compliant power management logic.

In addition to the features supported by Intel® ICH5, the Intel® ICH5R incorporates the Intel® RAID controller–the industry's first RAID (Redundant Arrays of Independent Disks) controller on a chipset, supporting RAID Level 0 in a two-drive configuration. This enhancement allows up to 300 MB/s bandwidth on data reads and writes through data striping.

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# 2 Highlights

The ICH5 has been designed to meet the needs for today's applications and the increased demands of future applications. In this section, several key ICH5 features and enhancements will be highlighted: Serial ATA, Intel RAID controller support (ICH5R only), USB 2.0, and ASF controller.

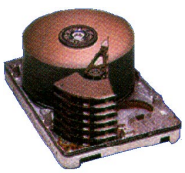
## 2.1 Serial ATA

The ICH5 and ICH5R enable next generation Serial ATA drives by integrating a dual-port Serial ATA controller. The ICH5 supports up to two SATA devices, providing an interface for SATA hard disks and other storage devices. The connection between motherboard and SATA storage device is accomplished by using a thin, flexible serial ATA cable. Since Serial ATA connections are point-to-point, the two SATA channels can have independent timings resulting in transfers occurring with no shared bandwidth. The individual channels can support Serial ATA transfers up to 1.5 Gb/s (150 MB/s), allowing headroom for ever-increasing Hard Disk Drive (HDD) media rates. The SATA controller can be configured to the standard primary and secondary channels, or with proper software support, can be configured as a Native IDE controller.

ICH5's Serial ATA implementation offers several advantages over Parallel ATA Technology:

- Point-to-point connection topology ensures dedicated 150 MB/s per device
- Dual controllers allow independent operation of each device
- Thinner, longer cables for easier routing and improved airflow in system chassis
- New connector design for easier installation and better device reliability
- CRC error checking on all data and control information

Integrating this controller into the ICH5 enhances the longevity of the platform. In addition, an integrated solution can help alleviate PCI bus bottlenecks caused by using discrete SATA solutions. Serial ATA extends beyond the theoretical limits of the Parallel ATA bus, supporting usage models such as digital video production, digital audio storage and recording, high-speed file sharing, and other data intensive applications.



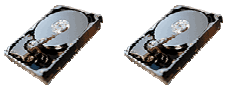
With only seven wires in the cable, clutter and space savings is achieved inside the system compared to an 80-pin Ultra ATA cable. Four of the wires are used for signaling, and the other three wires are ground used to minimize impedance and crosstalk. In addition, the 40-pin dual header for Ultra ATA can be replaced with 7-pin SATA connector taking up one-sixth the area on the system board for ease of routing.

Using a point-to-point connection topology, SATA reduces the effort of drive setup needed when using Parallel ATA. When a second SATA drive is added to the system, no configuration is needed. SATA eliminates the need for jumpers because there is one cable for each drive. No more figuring out which device is the master or slave.

The ICH5 SATA controller is designed to support hot swap when enabled with a notification mechanism and proper BIOS and operating system support. When a notification mechanism is used, a device can be safely powered down by software, and the port can then be powered off, allowing removal and insertion of a new device while the system is still on.

## 2.2 Intel® ICH5R with Intel® RAID Technology

In addition to the features of ICH5, the ICH5R I/O controller hub includes an integrated RAID controller that utilizes the dual Serial ATA ports for a high-performance RAID Level 0 configuration with a maximum theoretical transfer rate of 300 MB/s. By integrating the Intel RAID controller into the I/O controller hub, there are no PCI bandwidth limitations (133 MB/s) nor any loss of PCI resources (request/grant pair, PCI slot) that would typically occur with discrete PCI RAID solutions.



RAID Level 0 support is enabled by combining two Serial hard drives on the dual Serial ATA ports of ICH5R to achieve increased disk I/O performance. Intel RAID Technology on ICH5R requires the following components:

- 2 Serial ATA hard disk drives
- *Intel® Application Accelerator RAID Edition* software
- System BIOS that includes the Intel RAID Technology Option ROM

## 2.3 High-Speed USB 2.0

The ICH5 provides eight high-speed USB 2.0 ports, providing 40 times the bandwidth of full-speed USB. Each of the ICH5's USB ports support high-speed, full-speed, and low-speed USB devices. To achieve this capability on all eight ports, the ICH5 includes an Enhanced Host Controller Interface (EHCI) controller and four Universal Host Controller Interface (UHCI) controllers. The EHCI controller supports high-speed USB signaling for data transfers up to 480 Mb/s on all eight ports. Each of the UHCI controllers supports full-speed and low-speed USB signaling on two of the ports. When a device is plugged in, the ICH5's port routing logic will differentiate whether a high-speed USB device or a classic USB device is connected, and configures the appropriate UHCI or EHCI to take command of the device.

## 2.4 Alert Standard Format (ASF) Management Controller

Integrating an Alert Stand Format controller is one of several enhancements that have been made to the ICH5. By adding an ASF controller to the integrated LAN controller, interface system-monitoring devices can communicate through the integrated LAN controller to the network. This means remote manageability and system hardware monitoring are made possible using ASF.

The ASF controller can collect and send various information from system components such as the processor, chipset, BIOS and sensors on the motherboard to a remote server running a management console. The controller can also be programmed to accept commands back from the management console and execute those commands on the local system.

Some examples of ASF alerting capabilities include monitoring system health information, such as BIOS messages, POST alerts, OS failure notifications, and system heartbeat signals to indicate the system is accessible to the server. Also included are system environmental notifications such as thermal, voltage and fan alerts, which the ASF controller can send as proactive warnings that something is wrong with the hardware. ASF can also monitor physical tampering by providing messages such as “cover tampered” to notify of potential system break-ins and processor or memory theft. Remote-control capabilities allow remote power-up, power down, power cycle, reset or reboot. If necessary, the system can be commanded to reboot to multiple boot paths. The system can also be pinged to ensure that it is on the network and running correctly.

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# 3 Additional Features

ICH5 includes a variety of other enhancements and new functions to improve the platform performance, reduce costs, and add functionality. Some of those features are described here:

## 3.1 Hub Architecture

The ICH5's hub interface architecture ensures that the I/O subsystem, both PCI and the integrated I/O features (SATA, IDE, AC '97, USB, etc.), receive the bandwidth necessary for peak performance.

## 3.2 AC '97 2.3 Controller

The ICH5 integrates an *Audio Codec '97 Component Specification, Version 2.3* controller that can be used to attach an audio codec (AC), a modem codec (MC), an audio/modem codec (AMC) or a combination of ACs and a single MC. The ICH5 supports up to six channels of PCM audio output (full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center, and Subwoofer, for a complete surround-sound experience. ICH5 has expanded support for up to three audio codecs on the AC-link.

In addition, an AC '97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC '97. The ICH5-integrated AC '97 controller allows up to three external codecs to be connected to the ICH5. The system designer can provide AC '97 modem with a modem codec, or both audio and modem with up to two audio codecs with a modem codec.

## 3.3 PCI Interface

The ICH5 provides a 33 MHz, 32-bit, PCI 2.3 implementation. The ICH5 integrates a PCI arbiter that supports up to six external PCI bus masters in addition to the internal ICH5 requests. This allows for combinations of up to six PCI down devices and PCI slots.

## 3.4 IDE Interface

The fast IDE interface supports up to four IDE devices providing an interface for IDE hard disks and ATAPI devices. The IDE interface supports Ultra ATA transfers up 100 MB/s. The ICH5's IDE system contains two independent IDE channels that can be electrically isolated. The two IDE channels can be configured to the standard primary and secondary channels (four devices).

## 3.5 LAN Controller

In conjunction with the Intel® 82562 family of products, the ICH5's integrated LAN provides a 32-bit PCI device and a 10/100 Ethernet controller. Its bus master capabilities enable the component to process high-level commands and perform multiple operations; this lowers processor utilization by off-loading communication tasks from the processor. Two large transmit and receive FIFOs of 3 KB each help prevent data underruns and overruns while waiting for bus accesses. This enables the integrated LAN controller to transmit data with minimum interframe spacing (IFS).

## 3.6 System Management Bus (SMBus 2.0)

ICH5 provides an SMBus 2.0 Host Controller for the CPU to initiate communications with SMBus peripherals. In addition, ICH5 is also capable of operating in a mode in which it can communicate with $I^2C$ compatible devices. The ICH5 SMBus includes a slave interface which allows an external master to write or read to the ICH5 using the Host Notify Protocol. ICH5's SMBus also implements hardware-based Packet Error Checking for data robustness and the Address Resolution Protocol (ARP) to dynamically provide address to all SMBus devices.

# 4 Appendix

## 4.1 Related Documents

| Title | Location |
|---|---|
| *Intel® 82801EB I/O Controller Hub 5 (ICH5) and Intel® 82801ER I/O Controller Hub 5R (ICH5R) Datasheet* | http://developer.intel.com/design/chipsets/datashts/252516.htm |
| *Audio Codec '97 Component Specification, Version 2.3* | http://developer.intel.com/labs/media/audio/ |
| *Intel® 82801EB (ICH5) Serial ATA Controller Programmer's Reference Manual (PRM)* | http://developer.intel.com/design/chipsets/manuals/252671.htm |
| *Intel® 82801EB (ICH5), 82801ER (ICH5R), 82801DB (ICH4), 82801CA (ICH3), 82801BA (ICH2), 82801AA (ICH), and 82801AB (ICH0) IDE Controller Programmer's Reference Manual* | http://developer.intel.com/design/chipsets/manuals/298600.htm |
| *Intel® 82801EB (ICH5), 82801ER (ICH5R), and 82801DB (ICH4) Enhanced Host Controller Interface (EHCI) Programmer's Reference Manual (PRM)* | http://developer.intel.com/design/chipsets/manuals/298656.htm |
| *Intel® 82801EB (ICH5) I/O 82801ER (ICH5R), and 82801DB (ICH4) Controller Hub: AC '97 PRM, Product Reference Manual* | http://developer.intel.com/design/chipsets/manuals/252751.htm |